Claims

What is claimed is:

1. A microelectronic package array, comprising:

a first microelectronic package including a first carrier substrate having a first die side and a first non-die side, a first die electrically coupled to the first die side, and a land pad on the first die side;

a second microelectronic package comprising a second carrier substrate having a second die side and a second non-die side, a second die electrically coupled to the second die side, and a bond pad on the second non-die side; and

an intermediate substrate having a first side and a second side, the first side being coupled to the first die side of the first carrier substrate and the second side being coupled to the second non-die side of the second carrier substrate.

2. The microelectronic package array of claim 1, wherein the intermediate substrate further comprises

a substantially solid core having a first side and a second side;

an adhesive material disposed on the first side and second side of the core; and

a conductive riser disposed within the solid core.

3. The microelectronic package array of claim 2, wherein the intermediate substrate is mechanically bonded to the first die side of the first carrier substrate and the second non-die side of the second carrier substrate by the adhesive material.

4. The microelectronic package array of claim 3, wherein the adhesive material is a B-stage polymer.

5. The microelectronic package array of claim 3, wherein the core is a C-stage resin.

6. The microelectronic package array of claim 5, wherein the C-stage resin is reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate.

7. The microelectronic package array of claim 6, wherein the matrix is selected from a group including fiberglass cloth, composite fiber and non-woven fabric.

8. The microelectronic package array of claim 2, wherein the conductive riser is electrically coupled to the land pad of the first microelectronic package and the bond pad of the second microelectronic package.

9. The microelectronic package array of claim 8, wherein the conductive riser includes a first end and a second end having conductive plating disposed thereon, the first and second ends being electrically bonded to the land pad and the bond pad respectively by the conductive plating.

10. The microelectronic package array of claim 9, wherein conductive plating is selected from a group including leaded solder, lead-free solder and tin.

11. A system, comprising:

a system board;

a bus disposed on the system board to facilitate data exchange;

a memory configured to store data, the memory disposed on the system board and coupled to the bus;

a microelectronic package array disposed on the system board and coupled to the bus, the microelectronic package array comprising:

a first microelectronic package including a first carrier substrate having a first die side and a first non-die side, a first die electrically coupled to the first die side, and a land pad on the first die side;

a second microelectronic package comprising a second carrier substrate having a second die side and a second non-die side, a second die electrically coupled to the second die side, and a bond pad on the second non-die side; and

an intermediate substrate coupled to the first die side of the first carrier substrate and the second non-die side of the second carrier substrate.

12. The system of claim 11, wherein the intermediate substrate further comprises

a substantially solid core having a first side and a second side;

an adhesive material disposed on the first side and second side of the core; and

a conductive riser disposed within the solid core.

13. The system of claim 12, wherein the intermediate substrate is mechanically bonded to the first die side of the first carrier substrate and the second non-die side of the second carrier substrate by the adhesive material.

14. The system of claim 13, wherein the adhesive material is a B-stage polymer.

15. The system of claim 13, wherein the core is a C-stage resin.

16. The system of claim 15, wherein the C-stage resin is reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate.

17. The system of claim 16, wherein the matrix is selected from a group including fiberglass cloth, glass fiber carbon fiber and non-woven fabric.

18. The system of claim 12, wherein the conductive riser is electrically coupled to the land pad of the first microelectronic package and the bond pad of the second microelectronic package.

19. The system of claim 18, wherein the conductive riser includes a first end and a second end having conductive plating disposed thereon, the first and second ends being electrically bonded to the land pad and the bond pad respectively by the conductive plating.

20. The system of claim 19, wherein conductive plating is selected from a group including leaded solder, lead-free solder and tin.

21. A method for fabricating a microelectronic package array, comprising:

providing a first microelectronic package having a first carrier substrate with a first die side and a first non-die side, and a plurality of land pads disposed on the first die side;

providing a second microelectronic package having a second carrier substrate with a second die side and a second non-die side, and a plurality of bond pads disposed on the second non-die side;

placing an intermediate substrate having a plurality of conductive risers disposed therein on the first die side of a the first carrier substrate;

placing the second carrier substrate on the intermediate substrate with the second non-die side coming in contact with the intermediate substrate;

mechanically coupling the intermediate substrate to the first and second carrier substrates; and

electrically coupling the plurality of conductive risers with the plurality of land and bond pads.

22. The method of claim 21, wherein the method further comprises:

placing the microelectronic package array in a vacuum chamber;

creating a vacuum in the vacuum chamber;

applying heat to the microelectronic package array;

applying pressure to the microelectronic package array;

releasing the pressure; and

cooling the microelectronic package array.

23. The method of claim 22, wherein creating a vacuum comprises establishing a pressure of about less than ten kilo Pascals.

24. The method of claim 22, wherein applying heat comprises raising the temperature to about between 150 $^{\circ}C$ and 350 $^{\circ}C$.

25. The method of claim 22, wherein applying a pressure comprises increasing the pressure to a range between 0.5 mega Pascals and 10 mega Pascals.

26. The method of claim 21, wherein the intermediate substrate further includes a core having a first side and a second side, and an adhesive material disposed on the first side and the second side.

27. The method of claim 26, wherein the core is a C-Stage resin and the adhesive material is a B-stage polymer.